APPLICATION NOTE

The AU5790 single wire CAN transceiver is a line transceiver intended primarily for in-vehicle class B multiplexing applications. This device provides interfacing between a CAN data link controller and a single wire physical bus system with ground return.

AN2005
AU5790 Single wire CAN transceiver

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CONTENTS

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1. INTRODUCTION

The AU5790 single wire CAN transceiver is a line transceiver intended primarily for in-vehicle class B multiplexing applications. This device provides interfacing between a CAN data link controller and a single wire physical bus system with ground return.

This application note is intended to explain AU5790 functions and benefits, and to guide the user in applying the AU5790 in a vehicle network environment.

2. OVERVIEW

2.1 CAN

The Controller Area Network (CAN) is a serial communication protocol widely used in Automotive and Industrial applications for interconnecting control units, sensors, actuators, etc.

There are two relevant CAN message formats in use today. One is the standard message format which is defined in CAN Specification 1.2. The other one is the extended message format which is described in CAN Specification 2.0 Part B.

Primarily the two differ in that the standard message frame has 11 identifier bits, where the extended frame has 29 identifier bits.

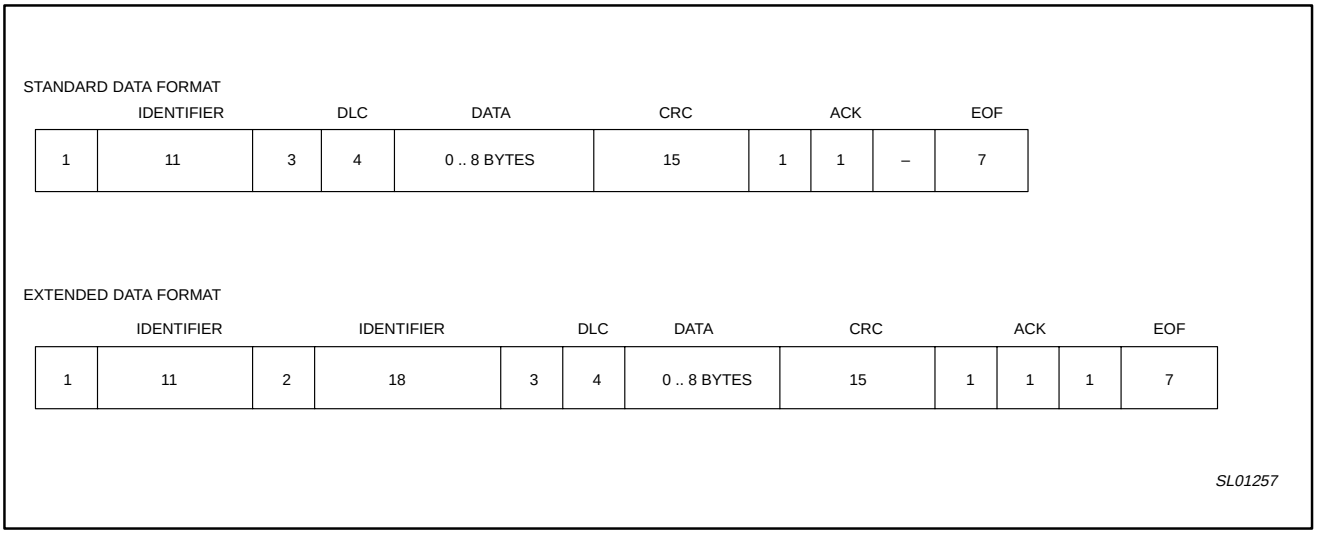


Figure 1. CAN message frames

2.1.1 Bit Timing and Propagation Delay

By the CAN bit timing definition, the Nominal Bit Time (NBT), with time duration $t_{bit,}$ consists of three non-overlapping segments: SYNC_SEG, TSEG1, and TSEG2, with time duration $t_{SYNC\_SEG,}$ $t_{seg1,}$ and $t_{seg2,}$ respectively, as shown in Figure 2. Each of these segments may be programmed to be an integral number of the Time Quantum (TQ), whose time duration, $t_{Q,}$ is derived from the oscillator. The sample point usually is located at the end of TSEG1.

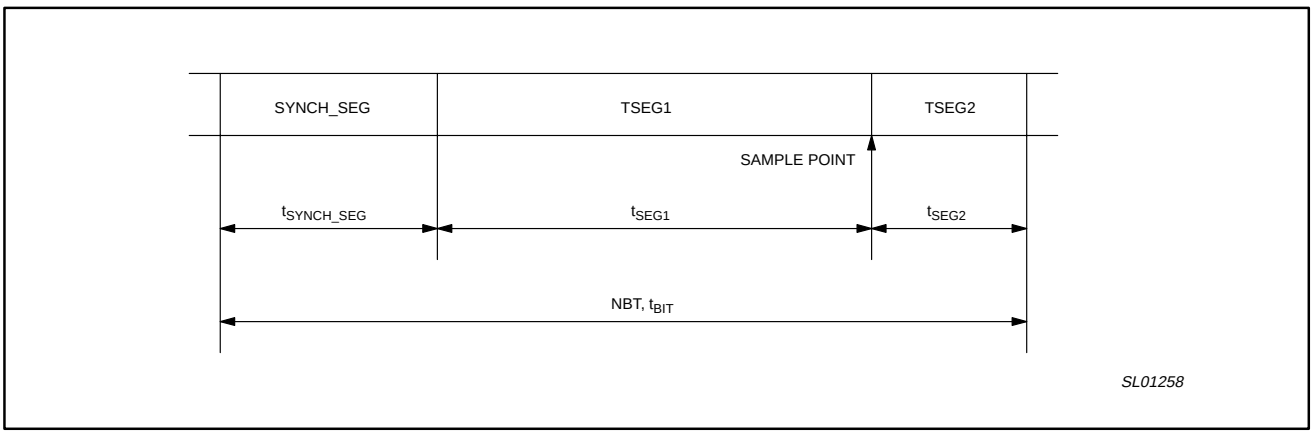


Figure 2. CAN bit time definition

Within CAN each node must synchronize to each other's message on the first recessive to dominant edge of the message and all the other recessive to dominant edges in the message waveform. Because each node has its own clock reference, the oscillator tolerance, Δf, will affect the bit time and the sample time, so Δf has big impact on the synchronization. Meanwhile, CAN supports arbitration and in-frame acknowledgment, which means after sending out a data bit the transceiver needs to read back the bus level, so the propagation delay between nodes in the network must be limited to guarantee synchronization.

The propagation delay from node A to node B includes all the device delays in the transmission path from A to B, CAN controller A delay time, transceiver A transmit delay, transceiver B receive delay, and bus line delay, etc. Since all nodes must receive each other's signal, and synchronize to it, then send them back during arbitration, the total propagation delay in the network should be the round trip delay.

Dietmayer and Overberg analyzed CAN bit timing requirements in detail in their SAE technical paper #970295[1]. By summarizing their analysis, we can find that in order to guarantee CAN bit time requirement, the total propagation delay has to satisfy following equations:

$$t_{prop}(max) < t_{bit} - t_{seg2} - (25t_{bit} - t_{seg2})^* \Delta f \quad (1)$$

$$t_{prop}(max) < t_{bit} - t_{seg2} - (25t_{bit} - t_{seg2})^* \Delta f + t_{prop}(min)/2 - t_Q (1- \Delta f) \quad (2)$$

The requirement on Equation (1) is more severe than that on Equation (2) if the minimum propagation delay is larger than $2^* t_Q$.

2.1.2 Arbitration

If no device is transmitting a message, the network bus is in a recessive state, and any device may start to transmit a message. If more than one device starts to transmit a message at the same time, only one device gets bus access successfully by bit arbitration using the identifier.

All devices on the bus are connected to the bus in a wired OR configuration. During arbitration, every device compares the read-back bus level with the transmitted data level. If these levels are the same, the transmission continues. If a device sends a recessive level, and reads back a dominant level, it has lost arbitration and has to stop sending any more bits, and becomes a receiver.

The following figure shows an arbitration example. Node 1, 2, and 3 start to send out message at the same time. At bit ID-23, node 2 sends a recessive level, but the readback bus level is dominant, thus node 2 loses arbitration and becomes a receiver. Node 1 loses its arbitration at bit ID-20. Node 3 finally wins bus access and continues message transmission.

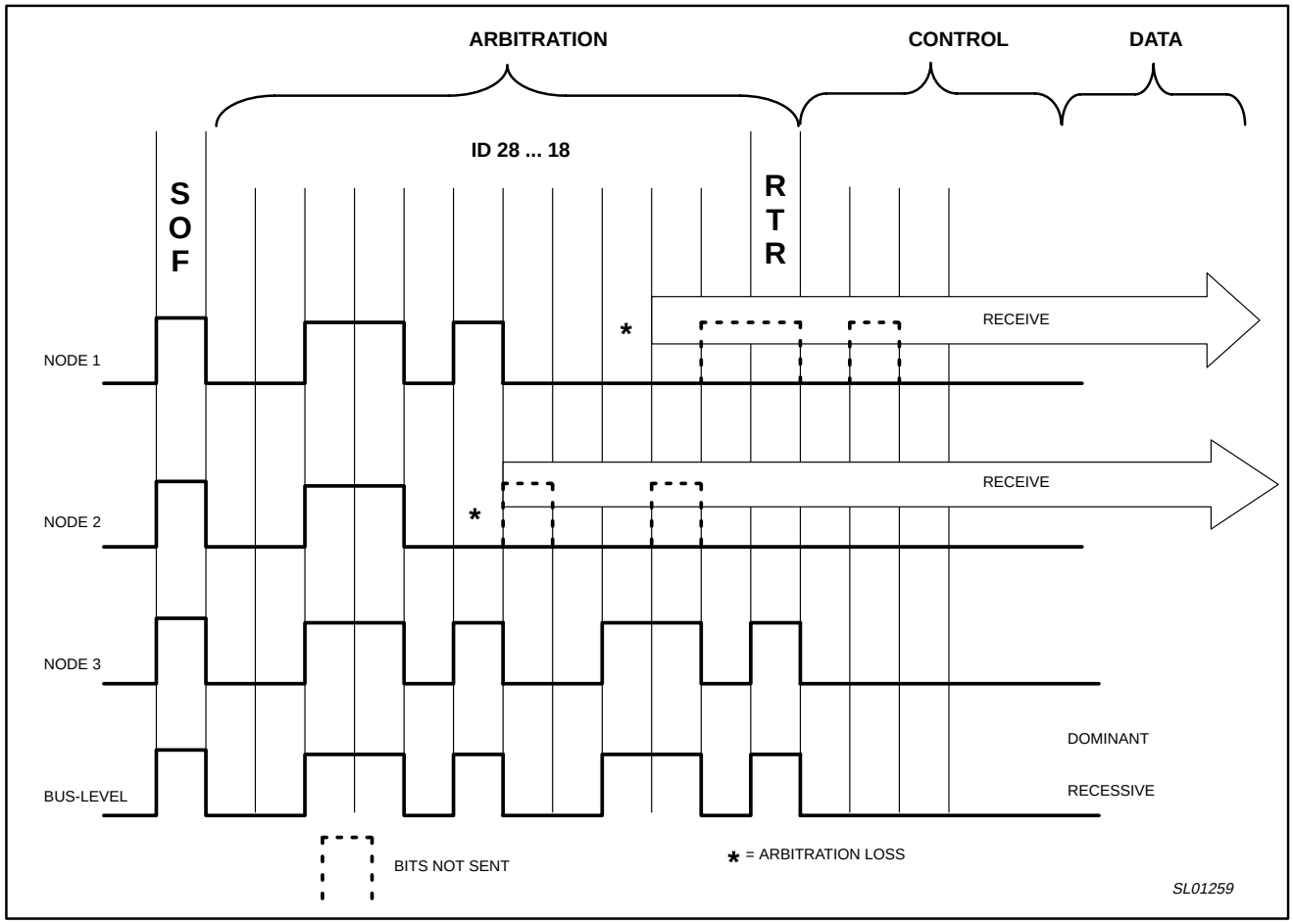


Figure 3. CAN bus arbitration

2.2 Single Wire CAN Transceiver

Dual wire CAN transceivers are being extensively used in high speed (~1 Mbps) and medium speed (~125 Kbps) applications where data transfer rate is the primary goal. The two wire approach lends itself well to high speed transmission while taking advantage of the inherent noise cancellation associated with balanced twisted pair medium implementations.

In cost sensitive applications as in body electronics, where data rates can be reduced below 50 Kbps, single wire solutions provide a good speed/cost alternative. In single wire systems EMC must be dealt with in the transceiver through wave-shaping to reduce frequency components above the data rate.

The fundamental difference in network topology between the various types of transceivers offered by Philips is shown below.

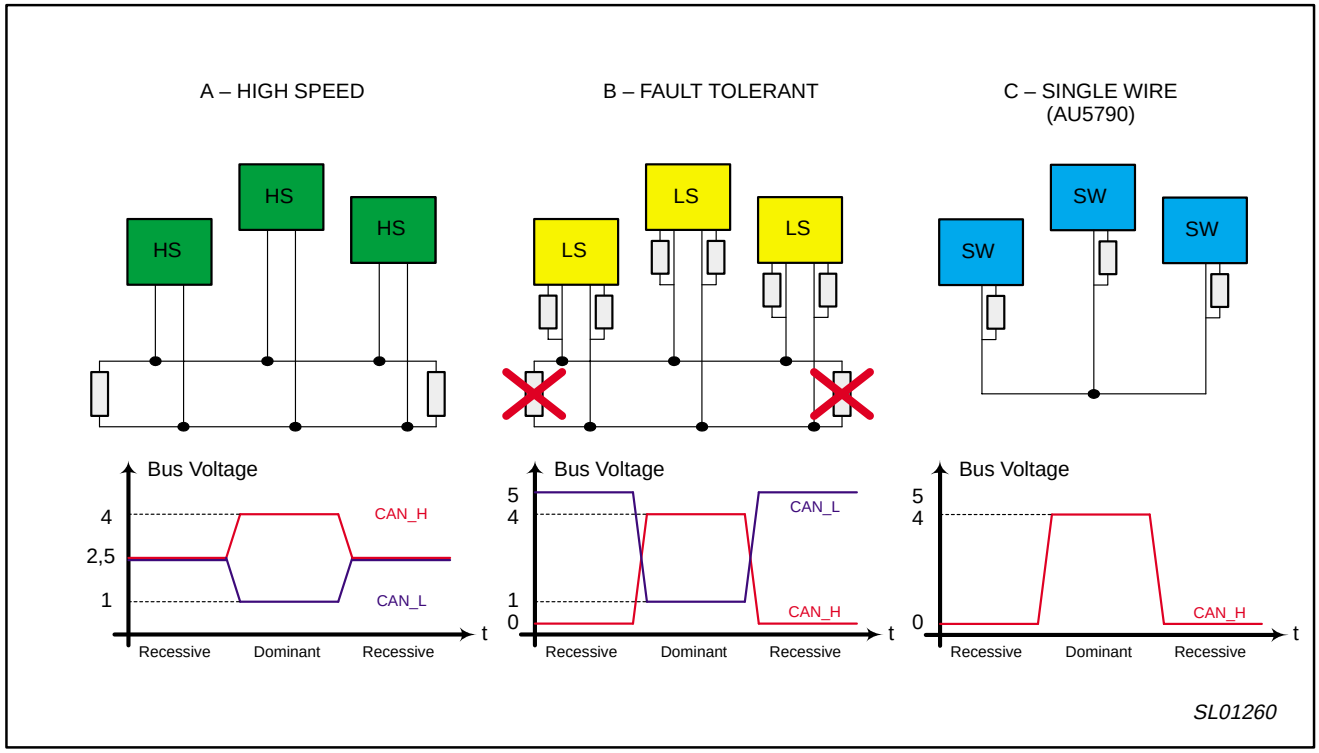


Figure 4. CAN transceivers comparison

Figure 4(a) is a high speed CAN network with termination resistor to set the recessive level.

In Figure 4(b) a fault tolerant CAN network eliminates termination resistors and permits communication to continue under some fault conditions. Resistors at each node set the recessive level.

The single wire CAN network shown at Figure 4(c) reduces the number of wires, and number of connectors or wire splices in half while also reducing wiring harness weight. Resistors at each node set the recessive level.

2.3 AU5790 in CAN Node Architecture

A CAN node can be subdivided into three layers, as shown in Figure 5.

The object layer is concerned with message filtering as well as status and message handing.

The transfer layer represents the kernel of the CAN protocol. It presents messages received to the object layer and accepts message to be transmitted from the object layer. The transfer layer is responsible for bit timing and synchronization, message framing, arbitration, acknowledgement, error detection and signalling, and fault confinement.

The physical layer actually transmits signals. The AU5790 is a physical layer interface device in a CAN structure.

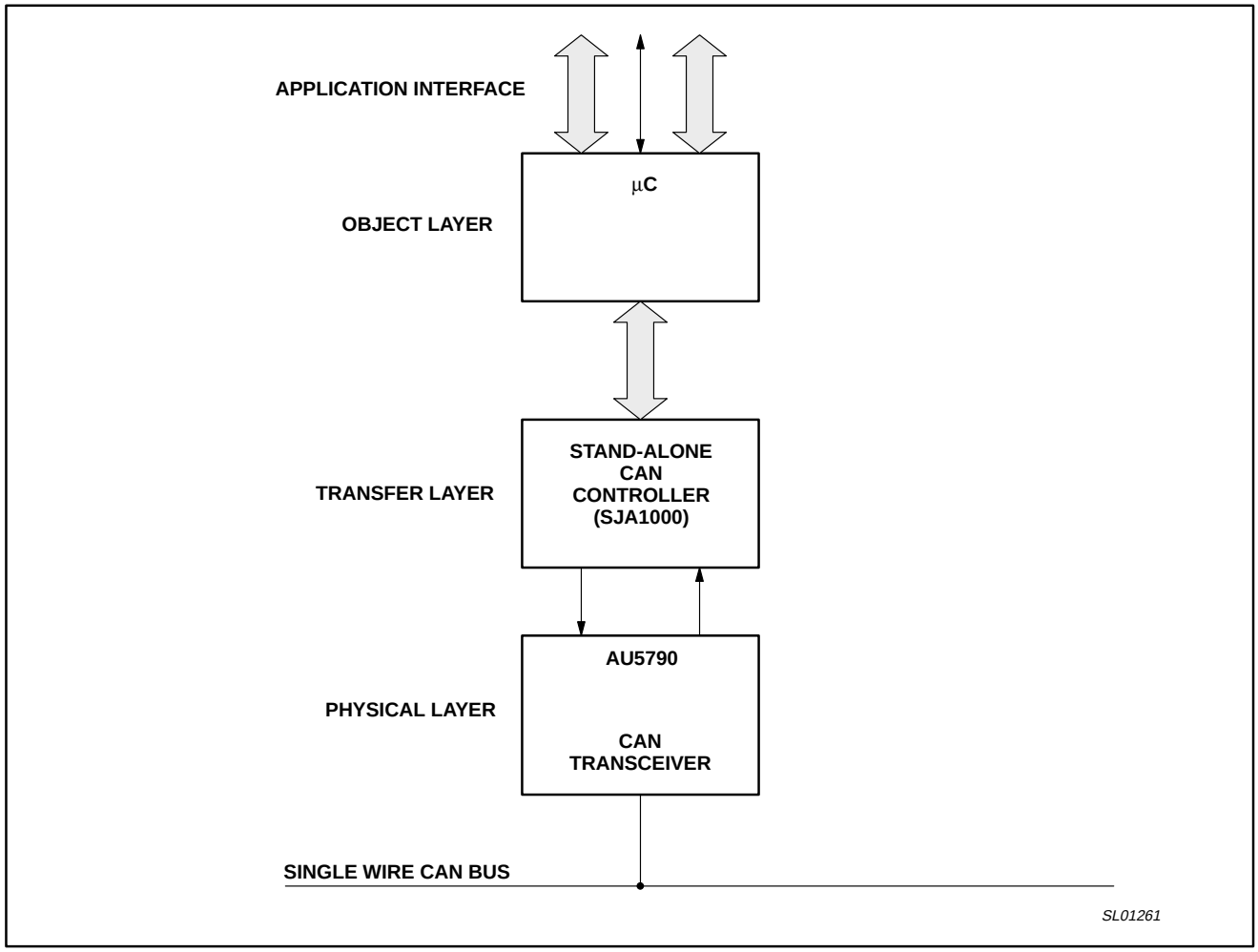


Figure 5. CAN node structure

3. AU5790 FEATURES

3.1 Feature list

- Supports in-vehicle class B multiplexing via a single bus line with ground return
- 33 kbps CAN bus transmission speed
- 83 kbps high-speed download mode
- Up to 32 bus nodes
- 70 μA power consumption in sleep mode
- Low electromagnetic emission due to output wave-shaping
- Direct battery operation with protection against load dump, jump start and transients
- Bus terminal protected against short-circuits and transients in the automotive environment
- Built in loss of ground protection
- Thermal overload protection
- Wake-up feature supports communication between control units even when network is in sleep state
- ± 8KV ESD protection on bus and battery pins

3.2 Block Diagram and Function Description

The AU7590 consists of several functional blocks shown in the block diagram below.

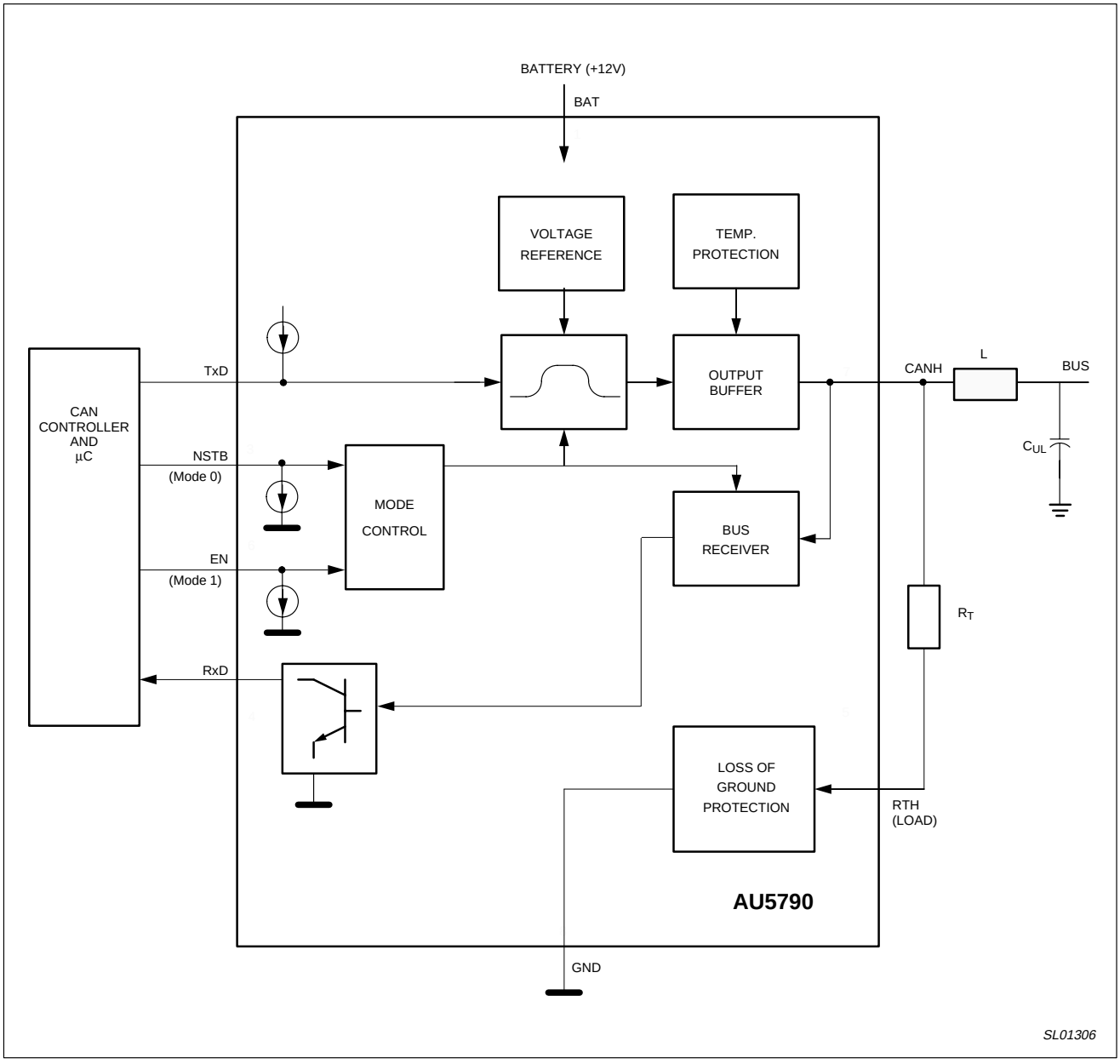


Figure 6. AU5790 block diagram

The protocol controller feeds the transmit data stream to the transceiver's TxD input. The AU5790 transceiver converts the TxD data input to a bus signal with controlled slew rate and wave-shaping to minimize electromagnetic emissions. The bus output signal is transmitted via the CANH in/output pin, which is connected to the physical bus medium. If TxD is low, then a typical voltage of 4 V is output at the CANH pin. If TxD is high then the CANH output is pulled passive low via the local bus load resistance R_T. The physical bus lines for all transceivers on the bus are connected in a wired-OR configuration, therefore the bus will be at a dominant level unless all nodes in network are passive.

To provide protection against a disconnection of the module ground wire the resistor R_T is connected to the RTH pin of the AU5790. The RTH pin is connected to ground via the loss of ground protection circuit in the AU5790. By providing this switched ground pin, no current can flow from the floating module ground to the bus via load resistor R_T.

The bus receiver detects the data stream at the bus line. The data signal is output at the RxD pin, which should be connected to a CAN controller. If the bus level is recessive, i.e. all transmitters are passive, then RxD is floating or High with external pull-up resistance. If the bus

level is dominant, i.e. at least one transmitter is active, then RxD is Low. The RxD is an open drain output, and needs an external pull-up resistance. To insure the RxD has the same voltage swing as other digital signal, the RxD pin should be pulled-up to the digital power supply Vcc. The AU5790 provides appropriate high frequency filtering to ensure minimum susceptibility against electromagnetic interference. Further enhancement is possible by applying an external inductor L and a capacitor C_{UL} at the CANH pin as shown in Figure 6.

The AU5790 features special robustness at its BAT and CANH pins. Hence the device is well suited for applications in the automotive environment. The BAT input is protected against 40V load dump, jump start conditions and all the conventional Automotive transients as defined in SAE J1113/ISO7637. In addition the CANH output pin is protected against ESD transients of at least 8KV without any external device protection. Protection against wiring fault conditions e.g. short circuit to ground or battery voltage is also included in the design.

A thermal protection shutdown function with hysteresis is incorporated aimed at protecting the device against system fault conditions leading to excessive operating junction temperature. In case the chip junction temperature reaches the trip point (>155 °C), the temperature protection circuit will turn-off the transmit function. The transmit function is available again after a small decrease of the junction temperature. The thermal shutdown hysteresis is about 5 °C.

NSTB and EN are mode control input pins. They are typically provided by a controller device. The AU5790 has four operation modes: sleep mode, wake-up mode, high-speed transmission mode, and normal transmission mode.

3.3 Operating Mode and Control

The microcontroller controls the transceiver's operating mode via the EN and NSTB pins. It is the microcontroller's responsibility to insure that the mode changes take place between the message frames. The following is the mode control summary table.

Table 1. Mode Control Summary

NSTB	EN	T_XD	Description	CANH	R_XD
0	0	don't care	sleep mode	0 V	float(high)
0	1	T_XD-data	wake-up mode	0 V, 12 V	bus state
1	0	T_XD-data	high-speed mode	0 V, 4 V	bus state
1	1	T_XD-data	normal mode	0 V, 4 V	bus state

Times that the transceiver needs to change its operation mode are shown in following table.

Table 2. Mode Switching Time

From Mode	To Mode	Mode Switching Time (μs)
Normal	High speed	<30
Normal	Wake-up	<30
Normal	Sleep	<500
High speed	Normal	<30
Wake-up	Normal	<30
Sleep	Normal	<50

3.3.1 Sleep Mode and Power Management

Battery power management is extremely important while there are more and more electronic components on the in-vehicle network. The AU5790 supports partial networking, i.e. individual nodes can communicate in normal and/or high-speed mode without disturbing the sleep nodes in the network.

If the NSTB and EN control inputs are both pulled low or floating, the AU5790 enters a low-power or "sleep" mode. This mode is dedicated to minimizing ignition-off current drain, to enhance system efficiency. In sleep mode, the typical quiescent current is 70 uA, and the transmit function is disabled, e.g. the CANH output is inactive even when TxD is pulled low.

Sleeping nodes will ignore normal and/or high-speed communication on the bus, i.e. for 4.0 V dominant bus level, the RxD is still floating or High. Sleeping nodes may be activated using the dedicated wake-up mode. An internal network active detector monitors the bus for any occurrence of higher voltage signal level, typically 12 V, on the bus line with normal battery levels. If such levels are detected, a message will be passed on to the CAN controller via the RxD output. Since the receive delay in sleep mode is much longer than that in normal or high speed mode, the first wake-up message may be lost within the system. The controller should switch the transceiver to normal mode after it receives the wake-up signal even though the message itself may be corrupt, otherwise the node will be back to sleep mode after the wake-up message.

3.3.2 Wake-up Mode and Bus Signal Levels

When NSTB is low and EN is high the AU5790 enters wake-up mode i.e. it sends data with an increased signal level. This will result in an activation of all sleeping bus nodes within the network.

A wake-up message has a much higher signal level than the normal and/or high-speed data. The following figure shows the transmitted, bus and receive signals. The wake-up signal has a 12 V dominant level on the bus line while the normal signal level is 4 V, as shown in Figure 7. Sleeping bus nodes will ignore normal 4.0 V dominant bus levels, and only respond to high voltage wake-up signals.

Since the thresholds of the receiver are different, the receive delay in sleep mode (T_{TrW-S}) is much longer than that in normal mode (T_{TrN}) in Figure 7. The first wake-up message may be lost within the system. But a wake-up message is not require to be received correctly by sleeping nodes. It is only required that all sleeping nodes detect this high voltage signal and set a High signal on RxD, and the controller may start the oscillator for its time base, set transceiver to normal mode, etc.

In the meantime this high voltage wake-up signal has the same delay time at the normal signal threshold voltage, 3 V typical, as the normal voltage signal. So the normal mode nodes still can interpret this high voltage signal correctly.

The high-speed and the wake-up features should not be active at the same time within the network.

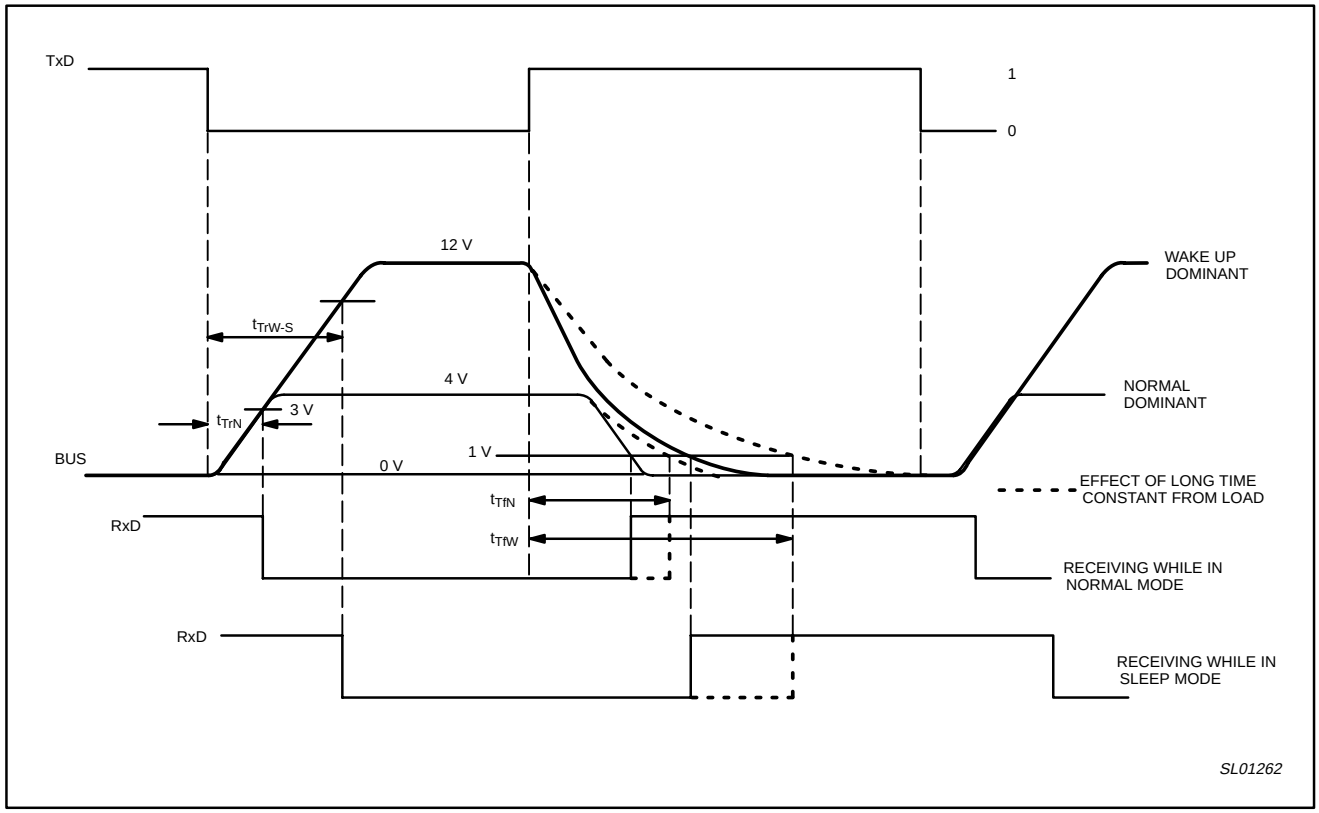


Figure 7. Bus voltage levels and delay time at normal and wake-up mode, not to scale

3.3.3 High Speed Data Download

The AU5790 also provides a high-speed transmission mode for software or diagnostic data download with bit rates up to 83 kbps. Usually an external node is attached to the network as the data source. If the NSTB input is pulled high and the EN input is low, then the internal wave-shaping function is disabled, i.e. the bus driver is turned on and off as fast as possible to support high-speed transmission of data. Consequently the EMC performance in this mode is degraded compared to the normal transmission mode. In high-speed transmission mode the AU5790 supports the same bus signal levels as in the normal mode.

For example, the user needs to download software from an external node or test tool.

1. Plug the external node on the bus, and the external node is in normal mode.
2. Sends ‘go to high speed mode’ message to all nodes. If some of nodes do not need to download the software, sends ‘go to sleep mode’ message to those nodes first, then sends ‘go to high speed mode’ message to the other nodes.
3. Controllers will set transceivers to high-speed mode (EN = 0, NSTB = 1) or sleep mode (EN = 0, NSTB = 0), respectively. The external node also goes to high-speed mode.
4. The external node sends data at the high speed bit rate.
5. The external node goes to normal mode and sends a ‘go to normal mode’ message to all nodes, or goes to wake up mode and wakes up all sleep nodes first, then put all nodes back to normal mode.
6. Unplug the external node.

The user should not allow high-speed mode nodes existing in the network at the same time with normal mode nodes, and wake-up mode nodes because it will cause bit timing errors.

3.3.4 Normal Mode and Wave-shaping

The AU5790 is in normal transmission mode when EN = 1, and NSTB = 1. In this mode, the transceiver sends a normal voltage signal onto the bus at a normal communication bit rate, typically 33.3 kbps.

Important contributors to the EM emissions are the rise and fall times during output transitions and the ‘corners’ of the voltage waveform. To minimize EM emissions, the AU5790 integrates a wave-shaping feature. The slew rate and the shape of the signal rising edges are controlled, as well as the onset of the falling edge. After the driver is off, the remaining fall time of the high to low transition is determined by the RC time constant of the total bus load.

3.4 Loss of Ground Protection

Figure 8 shows the currents flowing during normal operation. The modules ground is the same as the vehicle ground.

I_E I_E is the current flowing to ground through the other module circuits, represented by R_E.

I_T I_T is the current flowing to ground through the modules load resistor R_T.

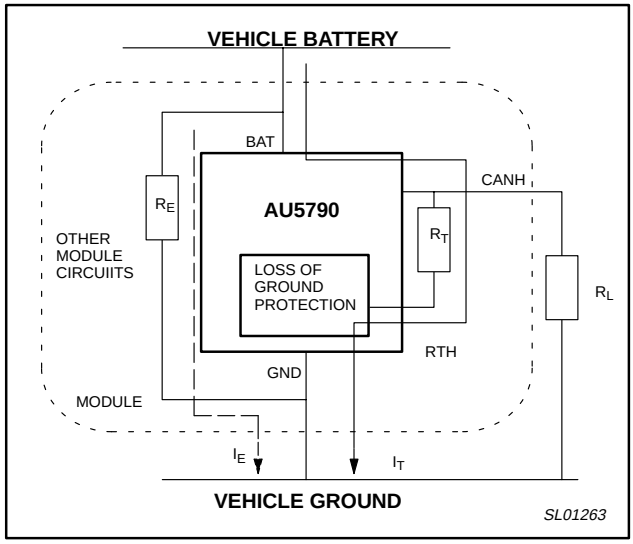


Figure 8. Current flow at normal condition

Figure 9 shows what happens when the ground connection between the module and the vehicle is broken, if there is no loss of ground protection. When the module looses its ground connection, any other ciruits between the module's internal ground and battery will act as a pull up to raise the module ground toward the battery level. These circuits are shown by their equivalent resistance, R_E. Without loss of ground protection, the current $_{IE}$ will flow through R_E and the termination resistor R_T which acts as pull up resistors, instead of the intended pull down. When the bus is in a recessive level, this current flowing through the load resistors of the other modules, will raise the voltage level on the bus. This will degrade bus noise margins, and potentially will corrupt proper data transmission,

I_E I_E is the current flowing to the bus through the other module circuits, represented by R_E and the termination resistor R_T

I_{CANLG} I_{CANLG} is the current flowing to the bus from the CANH driver during loss of ground without a loss of ground protection circuit. The actual current entering the bus from this node would be the sum of I_E and I_{CANLG}.

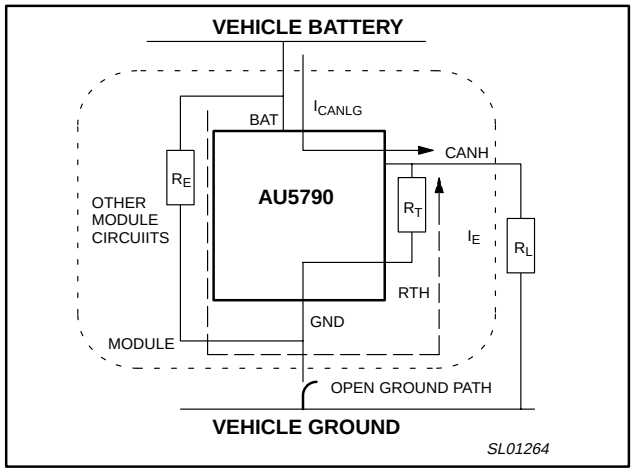


Figure 9. Current flow at module without loss of ground protection

Figure 10 shows operation when a loss of ground protect circuit is included. The aim of the loss of ground protection circuit is to open the current path from battery to the bus via the other module circuits, R_E, and through the load resistor R_T. Instead of connection to GND directly, RTH is connected to GND through a controlled switch. When the module looses its ground, the GND reference will float up toward the battery level. When the voltage drop between BAT and GND is less than ~5 V, the switch is opened and there is no current flow from this path. The AU5790 features a low leakage current of 50 μA max. to the bus during loss of ground. This low leakage current will keep the bus offset voltage sufficiently low to maintain proper bus levels for normal operation.

I_{CANLG} I_{CANLG} is the current flowing to the bus from the CANH driver during loss of ground, as tested, this is the sum of the leakage currents from both the CANH pin directly and from the RTH pin via the termination resistor, R_T.

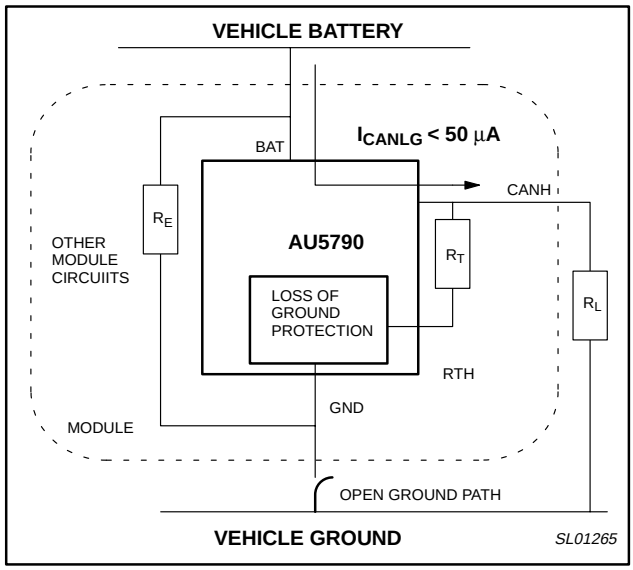
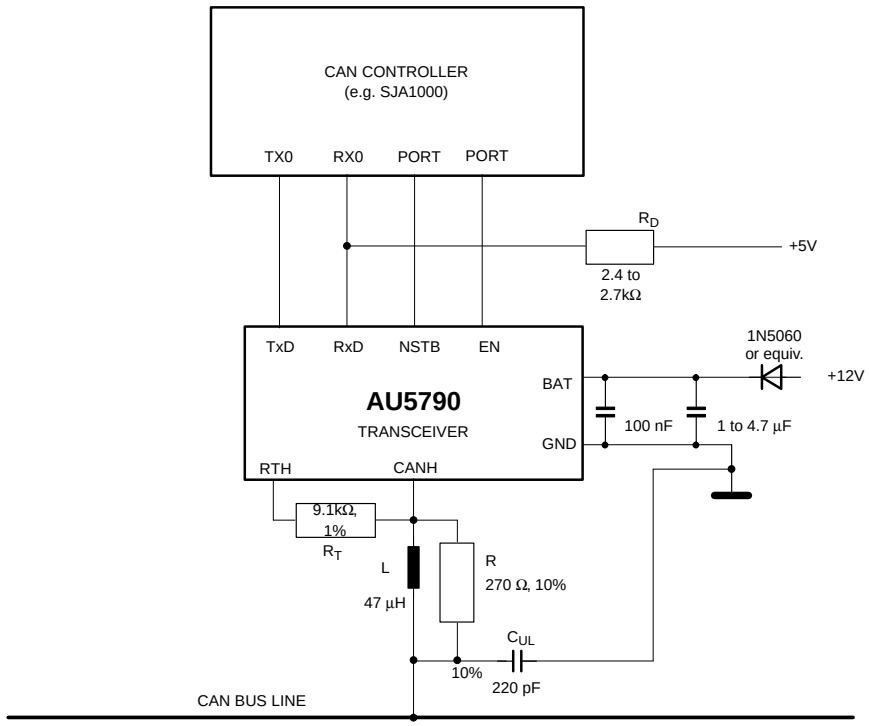


Figure 10. Loss of ground protection

4. APPLICATION INFORMATION

4.1 AU5790 Application Circuit



Note 1 TX0 should be configured to push-pull operation, active low; e.g., Output Control Register = 1E hex.
Note 2 Recommended range for the load resistor is 2k < R_T < 9.2k.

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Figure 11. AU5790 application circuit

The Microcontroller and CAN controller communicate with other nodes within the single wire can network via the transceiver.

The blocking diode between the battery and the AU5790 BAT pin protects the transceiver and all other module ICs from reverse battery voltages. It should support reverse breakdown voltages of > 100 V, and should have a forward drop of < 1V at the maximum current required by the module. The RxD pin is an open drain structure so it does not have an active pull up. A pull up resistor should be connected from RxD to the digital power supply V_{CC}, and a value of 2.4kΩ to 2.7kΩ should be used to meet the timing specified on the data sheet. This pull up allows the receive pin to drive the digital logic without having to supply V_{CC} to the transceiver.

R_T is the nodes load resistance within the module while C_{UL} is the unit load capacitance of the node.

The nodes loading components can have an effect on the modules EMC characteristics. An inductor, L, of 47 µH is required between the CANH pin and the bus. A damping resistor R in parallel can further improve EMC characteristics. The impact of the L and R on the EMC characteristics is dependent on the bus load and the frequency of interest. Figures 12 and 13 show the EM emissions with different combinations of total bus load R(L), total bus capacitance C(L) and the local nodes R and L values. With a light total load R(L) = 5.1 kΩ as shown in Figure 13, the series inductor, interacting with the load capacitance C(L) forms a tank circuit and including R decreases the Q of the tank circuit and hence the amplitude of the EME. If required to minimize EME at < 1 MHz, a damping resistor R of 270 Ω ±10% should be inserted in parallel with inductor L.

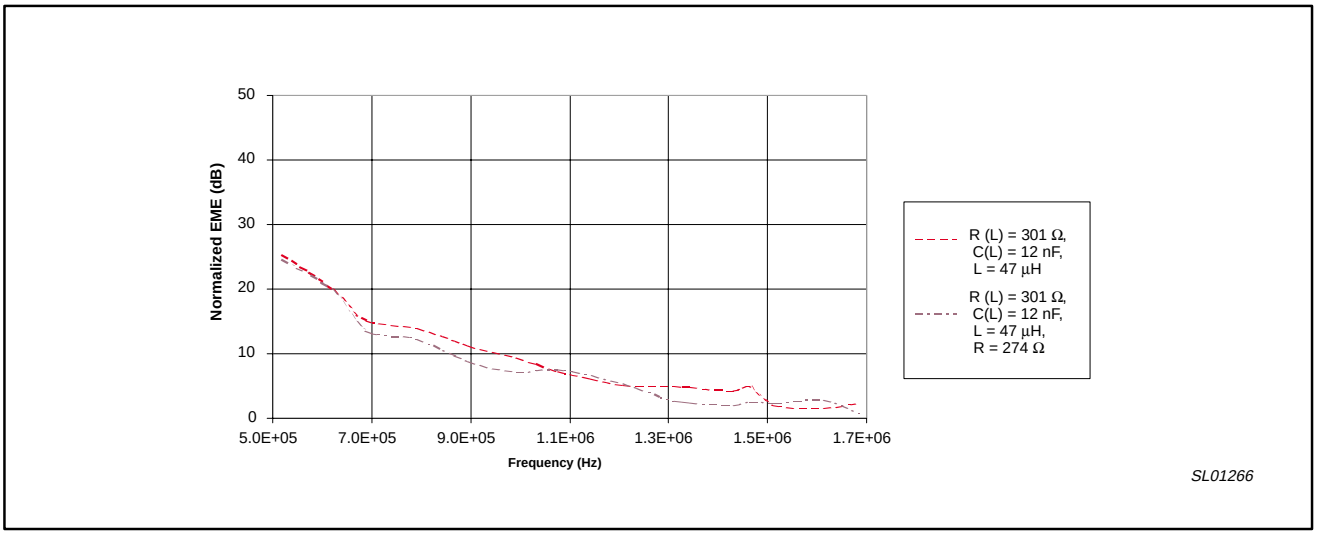

Figure 12. The influence of external components on EME with heavy load

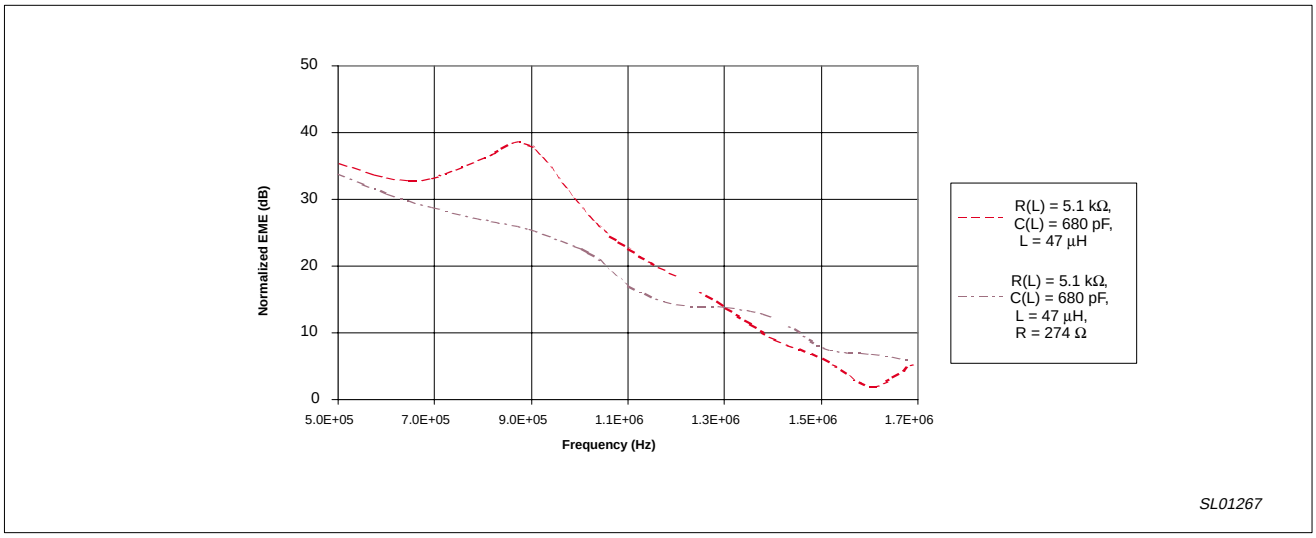

Figure 13. The influence of external components on EME with light load

4.2 Node and Bus Load Effects

For the AU5790 the termination resistor R_T is needed to pull down the bus line to the recessive level as default. C_{UL} is required to reduce interference caused by high frequency noise on the bus. A CAN node presents a R_T // C_{UL} load to the bus.

4.2.1 Basic Node Load

The basic node load R_T // C_{UL} is:

- C_{UL} = 220 pF (+/- 10%)
- 2 kΩ < R_T < 9.2 kΩ
  - For a network of 32 nodes, R_T = 9.1 kΩ (+/- 1%). A smaller value for R_T will result in violating the requirement for the CAN bus line total load, R_L.

4.2.2 CAN Bus Line Load

The total bus load R_L // C_L is:

- C_L < 13.7nF
  - C_L = sum of all C_{UL} + cable capacitance C_C
  - C_C = typically 100 pF/m * total length of all cable. Note the actual capacitance per meter is dependent on the cable chosen. Consult the wire specification for this value.
- 270 Ω < R_L < 9.2 kΩ
  - R_L is the all parallel equivalent of all the individual node resistors, R_T, between the CAN bus and ground.
  - The 270 Ω minimum bus load resistance is limited by the CANH output capability.
- 1µs < R_L * C_L < 4 µs
  - The bus time constant R_L * C_L determines the duration of the CANH signal's falling edge.
  - A small time constant may result in high EM emission. The bus time constant should not be less than 1µs in order to meet EMC requirements.
  - A large time constant may cause long transmit delay time, and violate CAN bit timing requirement. The bus time constant should not be more than 4 µs.

4.2.3 An Example of CAN Network

A CAN network may consist of both standard nodes and optional nodes, and node loads may be different. The user has to consider the minimum and maximum system, and all R_L, C_L, and R_L * C_L have to be within the range. Bus wiring capacitance tends to increase the time constant. A lower value of R_T in standard modules may be used to counterbalance this increase.

The following is a CAN network example:

- 5 standard nodes, R_T = 3.9 kΩ
- 0 to 20 optional nodes, R_T = 9.1 kΩ
- Node capacitance C_{UL} = 220 pF
- 40 meters wiring

For minimum system with 5 standard nodes:

- R_L = 3.9 kΩ / 5 = 780 Ω
- C_L = (220 pF * 5)+ (40 m * 100 pF/m) = 5.1 nF
- R_L * C_L = 3.98 µs

All parameters are within the requirement range, but the time constant R_L * C_L is near the maximum limit.

For maximum system with 5 standard and 20 optional nodes:

- R_L = 3.9 kΩ / 5 // 9.1 kΩ /20 = 287 Ω
- C_L = (220 pF * 25) + (40 m * 100 pF/m) = 9.5 nF
- R_L * C_L = 2.73 µs

All parameters are within the requirement range, but the load resistance R_L is near the minimum limit.

So this system is OK with all requirement. This example demonstrates that a lower value of R_T may be needed in standard nodes to keep the time constant within the spec, especially when the wiring in minimum system and maximum system are comparable, but the maximum number of 32 nodes can not be reached with this configuration.

4.3 Thermal Management

The AU5790 provides protection from thermal overload. When the IC junction temperature reaches the threshold (>155 °C), the AU5790 will disable the transmitter drivers, reducing power dissipation to protect the device. The transmit function will be available again after the junction temperature drops. The thermal shutdown hysterisis is about 5 °C.

In order to avoid this transmit function shutdown, care must be taken to not overheat the IC during normal operation. The relationship among the junction temperature, the ambient temperature, the dissipated power, and the thermal resistance can be expressed as:

$T_j = T_a + P_d * \theta_{ja}$

where: T_j is junction temperature (°C);

T_a is ambient temperature (°C);

P_d is dissipated power (W);

θ_{ja} is thermal resistance (°C/W).

4.3.1 Thermal Resistance

Thermal resistance is the ability of a subject to dissipate heat to its environment. In semiconductor applications, it is highly dependant on the IC package, PCBs, and airflow. Thermal resistance also varies slightly with input power, the difference between ambient and junction temperature, and soldering material, etc.

Figures 14 and 15 show the thermal resistance as a function of IC package and PCB configuration assuming no airflow.

The high/low conductance board is the JEDEC standard high/low effective thermal conductive test board. The JESD51-7 and EIA/JESD51-3 specifications are available from: http://www.jedec.org. The high conductance board contains two 1 oz thick Cu ground planes, and 2 oz (0.071 mm) thick Cu top and bottom trace layers. The low conductance board does not contain any ground planes, and has 2 oz (0.071 mm) thick Cu top and bottom trace layers. The very low conductance board is the PCB with EIA/JESD51-3 standard trace configuration, but the traces are 1 oz thick Cu instead of standard 2 oz Cu.

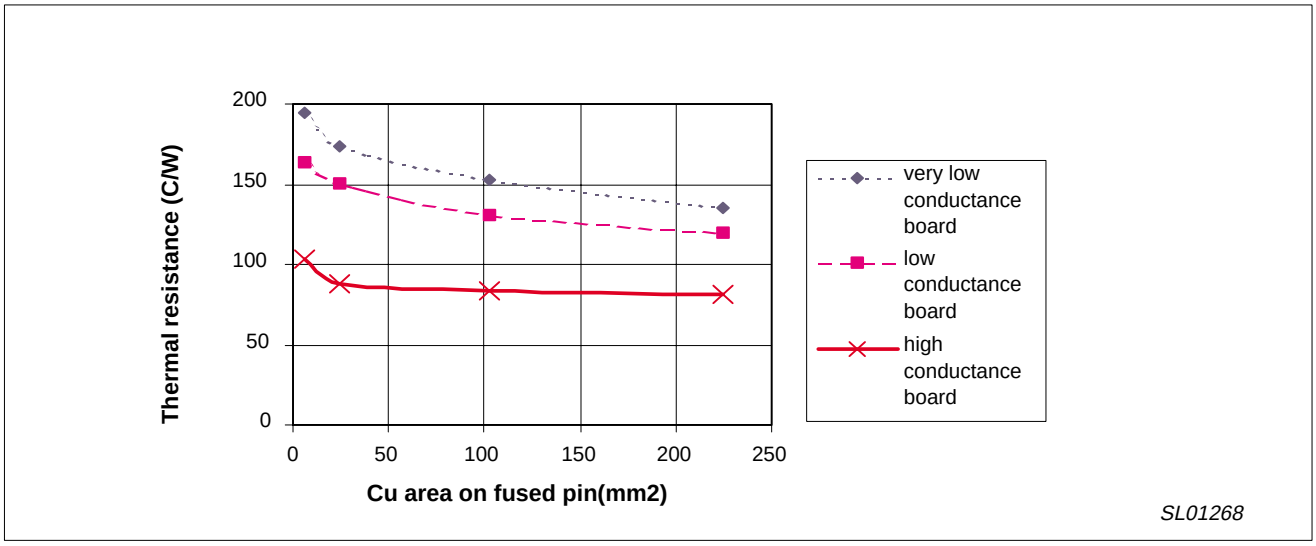

Figure 14. SO-8 thermal resistance vs. PCB configuration

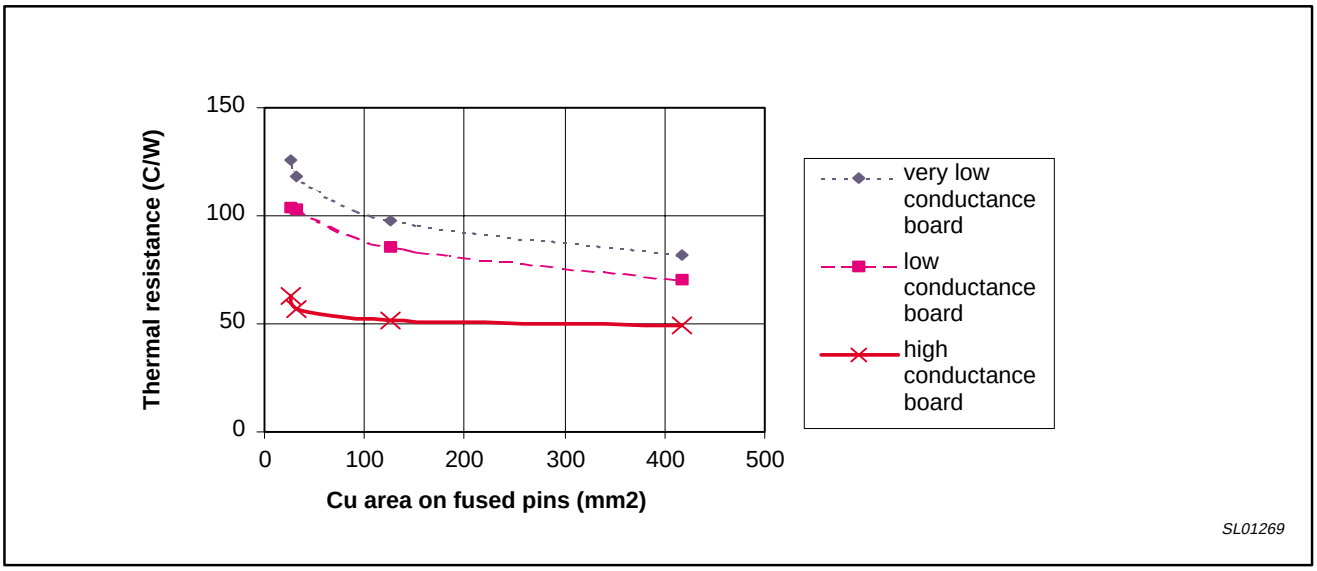

Figure 15. SO-14 thermal resistance vs. PCB configuration

Both the SO-8 and SO-14 have one or more pins which are directly connected, or fused, to the die bonding pad to provide an improved thermal path from the die to the pin. Normally the die pad and the lead frame are stamped from the same copper sheet during manufacture. Wire bonds connect from bonding pads on the die to the lead frame and the die attach pad supports the die. By making the copper continuous from the die attach pad to the lead frame these fused pins have lower thermal resistance than normal pins which rely on wire bonds to make electrical connections. Figure 16 shows sketches of both the SO-8 and SO-14 package construction. On the SO-8 package, pin 8 is directly fused with the die attach pad. On the SO-14 package all 4 corner pins are fused to the die attach pad. The thermal resistance from die to ambient can be further improved by putting an area of copper foil on the board connected to the fused pins. This copper area acts as a heat sink. The “Cu area on fused pin(s) (mm2)” shown on Figures 14 and 15 refers to the total area of copper connected to the fused pins.

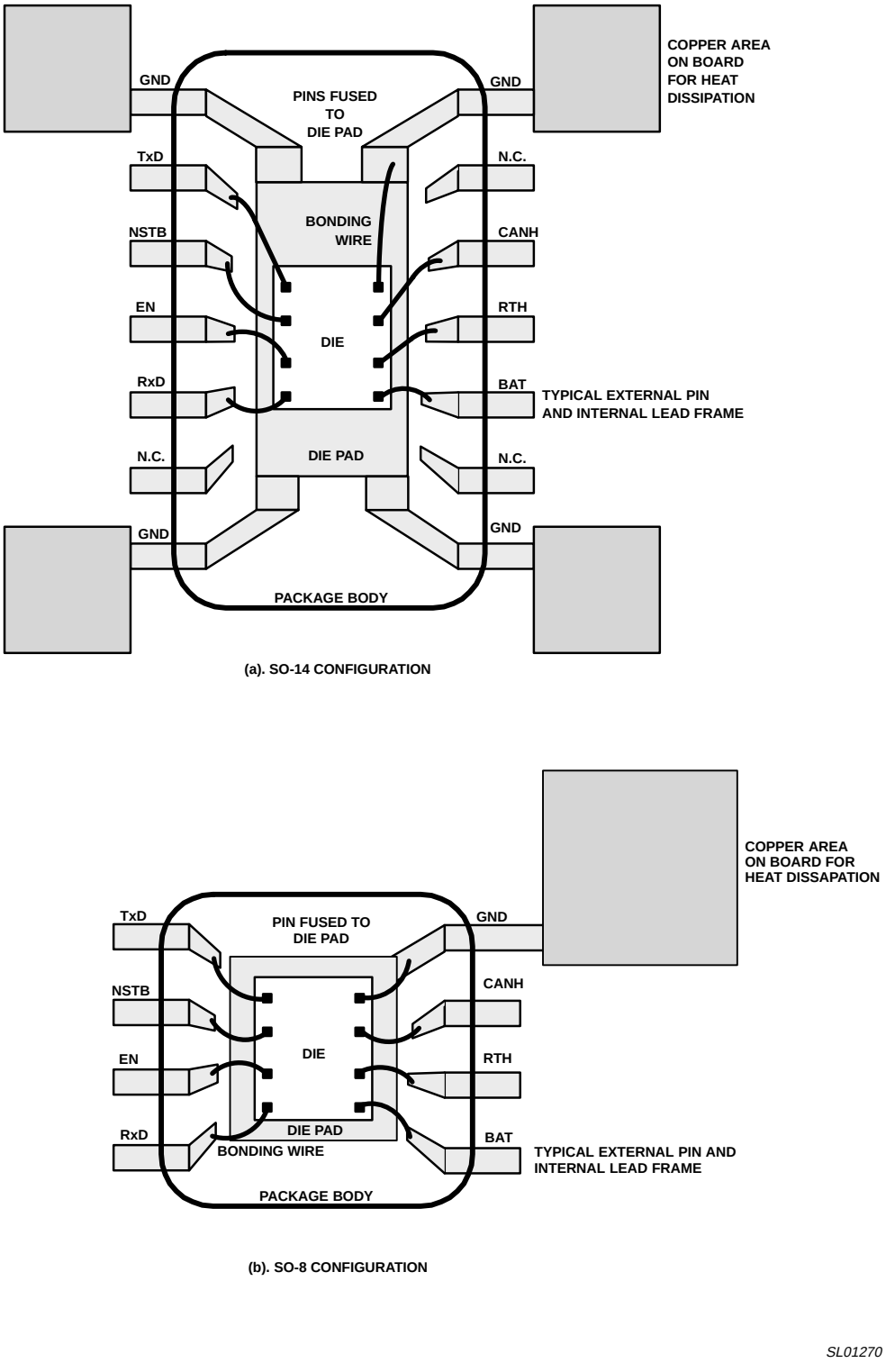

Figure 16. Package heat conductor configuration

4.3.2 Power Dissipation

The power dissipation of an IC is the major factor determining junction temperature. The AU5790 power dissipations in active and passive states are different. The average power dissipation is:

$$P_{tot} = P_{INT}*Dy + P_{PNINT} * (1-Dy)$$

where: P_{tot} is total dissipation power;

P_{INT} is dissipation power in an active state;

P_{PNINT} is dissipation power in a passive state;

Dy is duty cycle, which is the percentage of time that TxD is in an active state during any given time duration.

At passive state there is no current going into the load. So all of the supply current is dissipated inside the IC.

$$P_{PNINT} = V_{BAT} * I_{BATPN}$$

where: V_{BAT} is the battery voltage;

I_{BATPN} is the passive state supply current in normal mode.

In an active state, part of the supply current goes to the load, and only part of the supply current dissipates inside the IC, causing an incremental increase in junction temperature.

$$P_{INT} = P_{BATAN} – P_{LOADN}$$

where: P_{BATAN} is active state battery supply power in normal mode;

$$P_{BATAN} = V_{BAT} * I_{BATAN}$$

P_{LOADN} is load power consumption in normal mode.

$$P_{LOADN} = V_{CANHN} * I_{LOADN}$$

where: I_{BATAN} is active state supply current in normal mode;

V_{CANHN} is bus output voltage in normal mode;

I_{LOADN} is current going through load in normal mode.

$$I_{LOAD} = V_{CANHN}/R_{LOAD}$$

$$I_{BATN} = I_{LOAD} + I_{INT}$$

where: I_{INT} is an active state current dissipated within the IC in normal mode.

I_{INT} will decrease slightly when the node number decreases. To simplify this analysis, we will assume I_{INT} is fixed.

$$I_{INT} = I_{BATN} \text{ (32 nodes)} – I_{LOAD} \text{ (32 nodes)}$$

I_{BATN} (32 nodes) may be found in the DC Characteristics table.

A power dissipation example follows. The assumed values are chosen from specification and typical applications.

Assumptions:

V_{BAT} = 13.4 V
R_T = 9.1 kΩ
32 nodes
I_{BATPN} = 2 mA
I_{BATN} (32 nodes) = 35 mA
V_{CANHN} = 4.55 V
Duty cycle = 50%

Computations:

R_{LOAD} = 9.1 kΩ / 32 = 284.4 Ω
P_{PNINT} = 13.4 V × 2 mA = 26.8 mW
I_{LOAD} = 4.55 V / 284.4 Ω = 16mA
P_{LOADN} = 4.55 V × 16 mA = 72.8 mW
I_{INT} = 35 mA - 16 mA = 19 mA
P_{BATAN} = 13.4 V × 35 mA = 469 mW
P_{INT} = 469 mW - 72.8 mW = 396.2 mW
P_{tot} = 396.2 mW × 50% + 26.8 mW × (1-50%) = 211.5 mW

Additional examples with various node counts are shown in Tables 3, 4, and 5 for operation at 13.4 V, 18 V, and 26.5 V respectively.

Table 3. Power Dissipation At 13.4 V Battery Voltage Vs. Node Count

Nodes	R_L (Ω)	V_{BAT} (V)	I_{BATPN} (mA)	P_{PNINT} (mW)	V_{CANHN} (V)	I_{LOADN} (mA)	I_{BATN} (mA)	I_{INT} (mA)	P_{INT} (mW)	Dcycle	P_{tot} (mW)
2	4550	13.4	2	26.8	4.55	1	20	19	263.5	0.5	145.1
10	910	13.4	2	26.8	4.55	5	24	19	298.9	0.5	162.8
20	455	13.4	2	26.8	4.55	10	29	19	343.1	0.5	184.9
32	284.4	13.4	2	26.8	4.55	16	35	19	396.2	0.5	211.5

Table 4. Power Dissipation At 18 V Battery Voltage Vs. Node Count

Nodes	R_L (Ω)	V_{BAT} (V)	I_{BATPN} (mA)	P_{PNINT} (mW)	V_{CANHN} (V)	I_{LOADN} (mA)	I_{BATN} (mA)	I_{INT} (mA)	P_{INT} (mW)	Dcycle	P_{tot} (mW)
2	4550	18	2	36	4.55	1	20	19	355.5	0.5	195.7
10	910	18	2	36	4.55	5	24	19	409.3	0.5	222.6
20	455	18	2	36	4.55	10	29	19	476.5	0.5	256.3
32	284.4	18	2	36	4.55	16	35	19	557.2	0.5	296.6

Table 5. Power Dissipation At 26.5 V Battery Voltage Vs. Node Count

Nodes	R_L (Ω)	V_{BAT} (V)	I_{BATPN} (mA)	P_{PNINT} (mW)	V_{CANHN} (V)	I_{LOADN} (mA)	I_{BATN} (mA)	I_{INT} (mA)	P_{INT} (mW)	Dcycle	P_{tot} (mW)
2	4550	26.5	2	53	4.55	1	20	19	525.5	0.5	289.2
10	910	26.5	2	53	4.55	5	24	19	613.3	0.5	333.1
20	455	26.5	2	53	4.55	10	29	19	723	0.5	388
32	284	26.5	2	53	4.55	16	35	19	854.7	0.5	453.8

4.3.3 Selecting a Package and Board

In a user's application, the following are usually known or can be calculated from circuit parameters;

Tj(max) = 150 °C from the data sheet.
This is the maximum allowed junction temperature.

Ta(max) is known from the user's application.
Typically the maximum ambient temperature, Ta, it will be 85 °C for most body multiplexing nodes, however some nodes such as those in the instrument cluster may require operation at 105 °C and any nodes in the engine compartment will most likely require operation in a 125 °C ambient.

Pd(max) is the power dissipation for the worst case combination of load and supply voltage.
It can be calculated as described in the previous section for any application. Several summaries of calculated Pd are shown in Tables 3, 4, and 5 at the end of the previous section.

This leaves only the thermal resistance, θja, as an unknown. The thermal equation can be solved for θja.

$Tj = Ta + Pd*\theta ja$ Becomes; $\theta ja = (Tj–Ta)/Pd$

With θja calculated, Figures 14 and 15 may be used to determine a package and PC board configuration that will provide a thermal resistance, θja, less than the required value.

For example assume; θja(max) = 125 °C/W

Examining Figure 14 for the SO-8 package we find that a high conductance board with just the normal signal traces will provide approximately 100 °C/W and hence exceeds the requirements with margin to spare. The low conductance board will also work if 225-sq. mm of foil area is included on pin 8, the fused pin, to act as a heat sink providing approximately 120 °C/W. It can also be seen that the very low thermal conductance board will not support this application using an SO-8 package. If we now examine the SO-14 curves in Figure 15 we find even the very low conductance board will meet the needs of the application with minimal additional copper foil for heat dissipation, and the low and high conductance boards do not require any extra foil area.

For selected operating voltages Figures 17 through 22 shows plots that allow the user to select a board type if the number of standard nodes, operating voltage, and ambient temperature are known. These plots were created using the data and equations from the previous two sections. Select the plot for the operating voltage and package type being considered, and then find the intersection of the maximum node count and the highest ambient temperature required. Any curve which is above the intersection point represents a board type and possible area of heat dissipating copper foil which will provide a low enough thermal resistance to meet the applications needs. These plots assume all nodes use the normal unit load resistance of 9.1 kΩ, and insure that the junction temperature, Tj, will not exceed 150 °C.

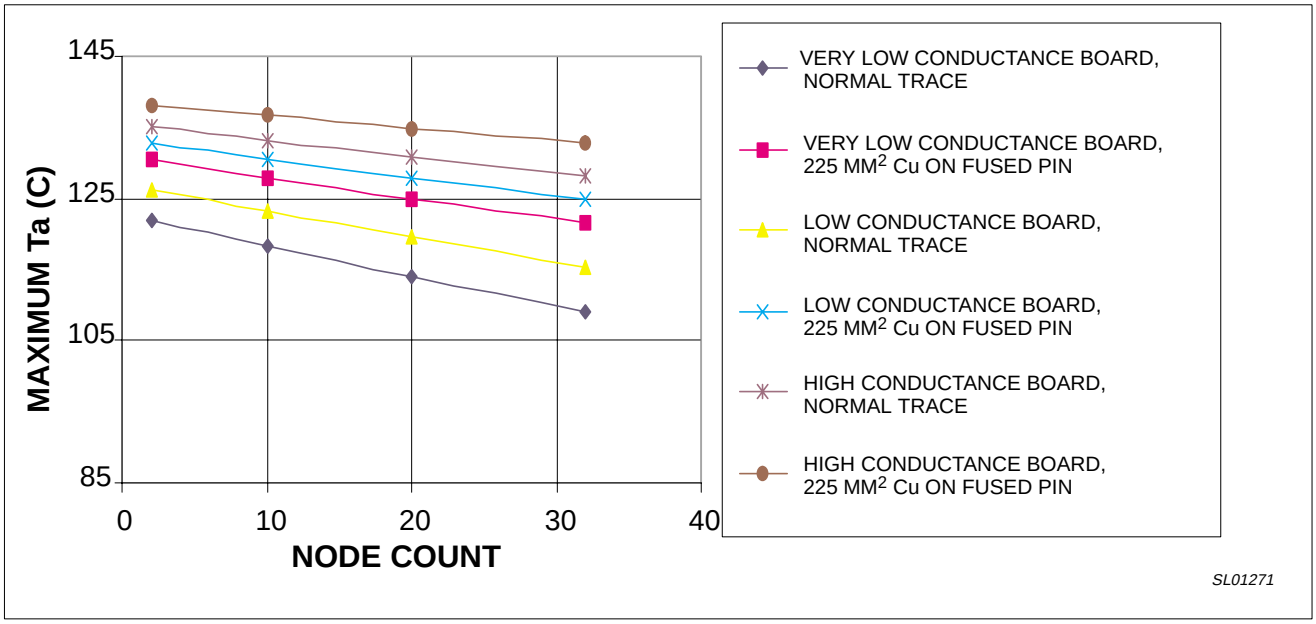

Figure 17. Maximum ambient temperature SO-8 may support vs. node count at 13.4 V battery voltage

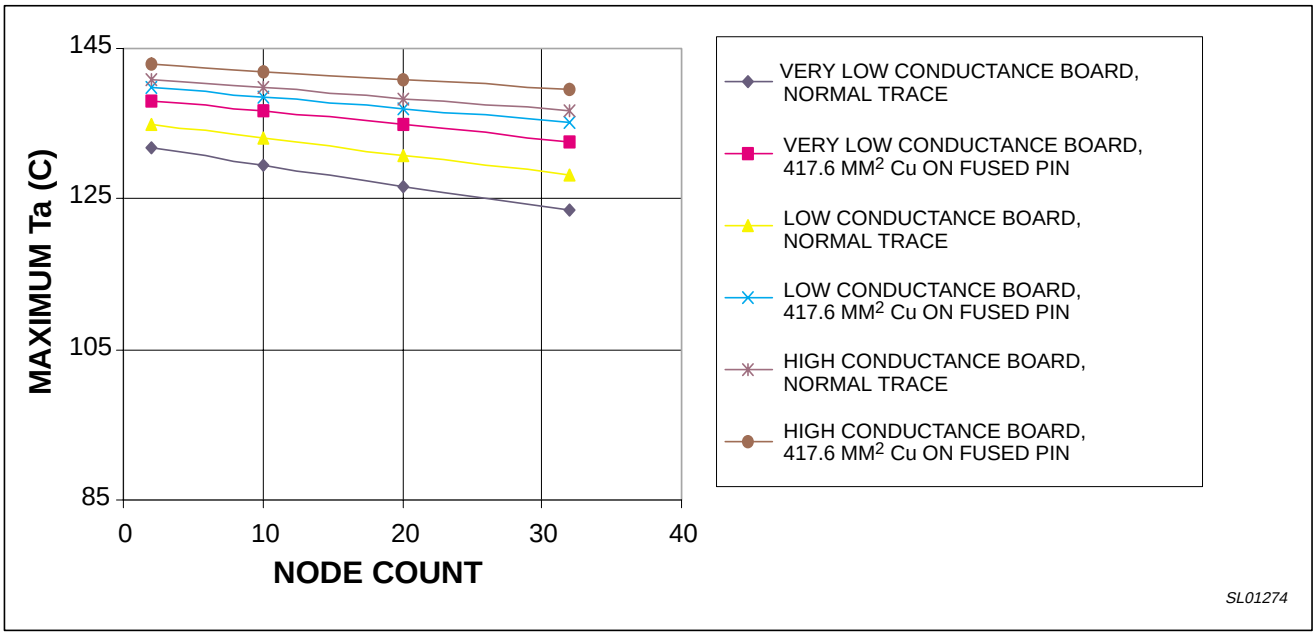

Figure 18. Maximum ambient temperature SO-14 may support vs. node count at 13.4 V battery voltage

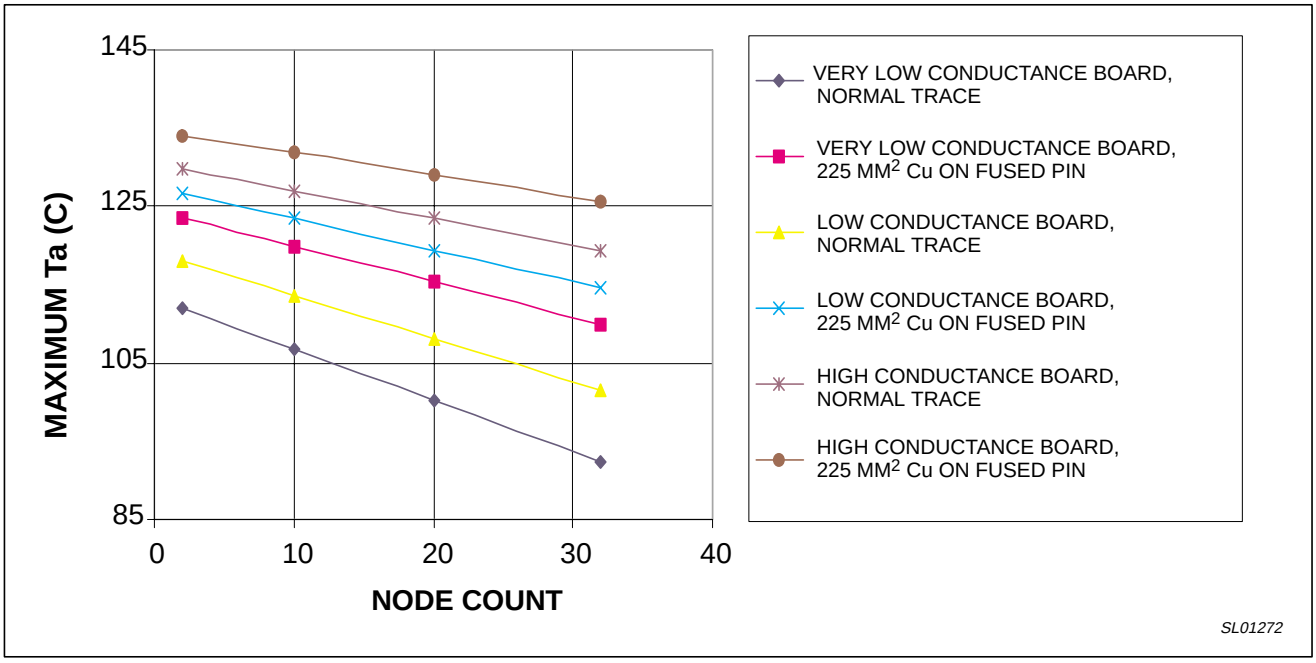

Figure 19. Maximum ambient temperature SO-8 may support vs. node count at 18 V battery voltage

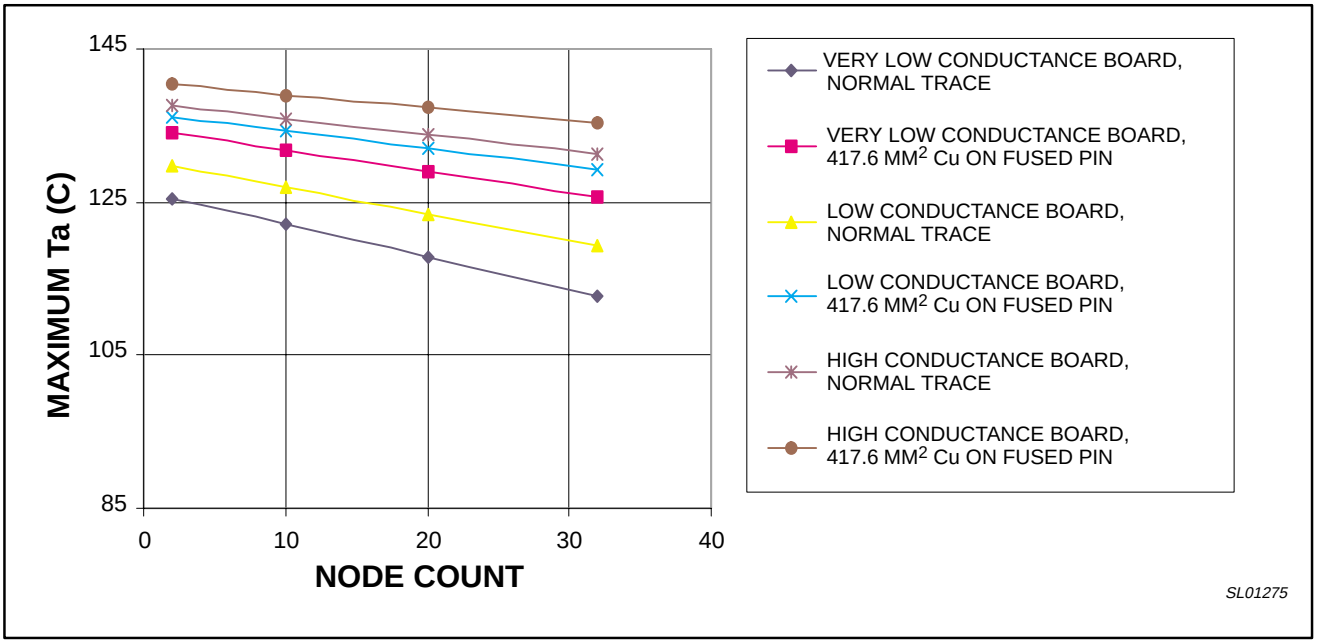

Figure 20. Maximum ambient temperature SO-14 may support vs. node count at 18 V battery voltage

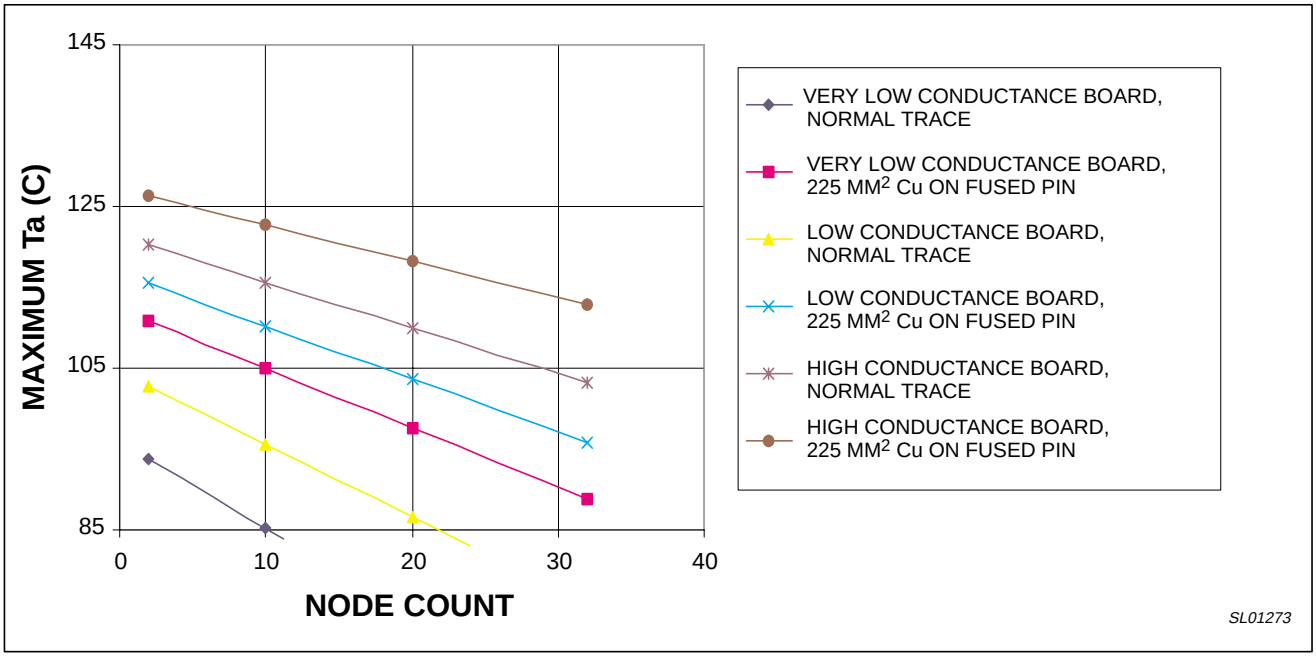

Figure 21. Maximum ambient temperature SO-8 may support vs. node count at 26.5 V battery voltage

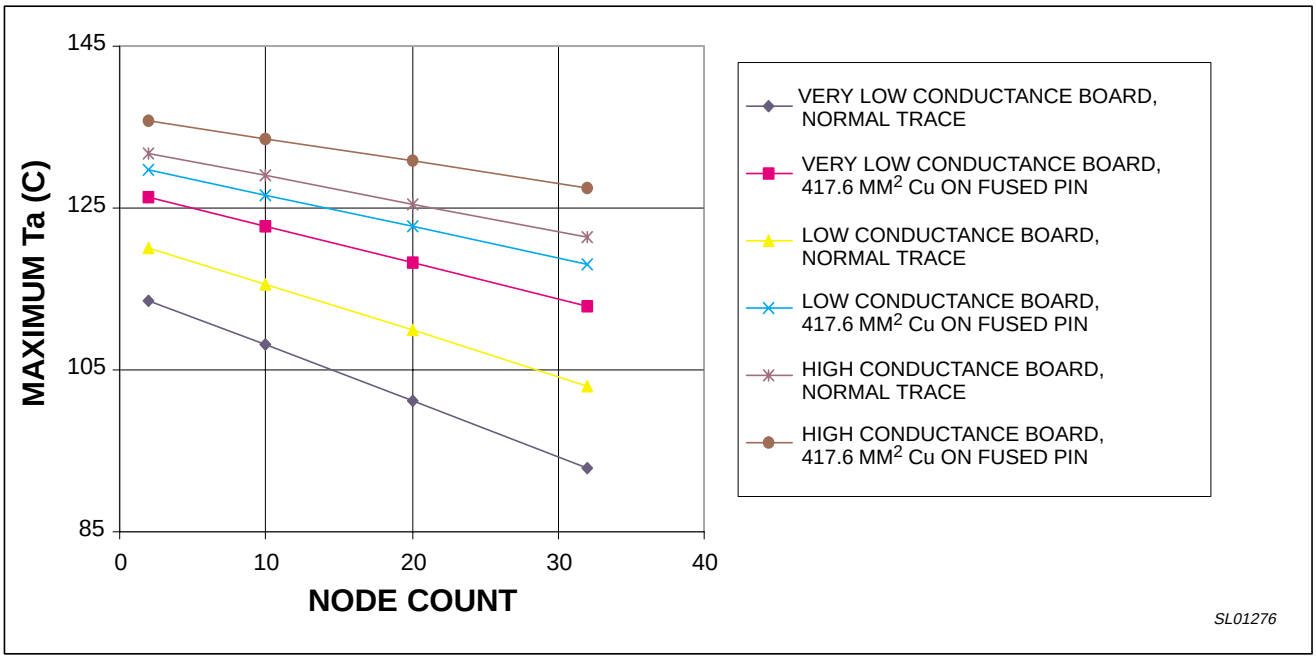

Figure 22. Maximum ambient temperature SO-14 may support vs. node count at 26.5 V battery voltage

Reference

[1] K. Dietmayer, K. W. Overberg, 'CAN Bit Timing Requirements', SAE Technical Paper Series, #970295.

NOTES

AU5790 Single wire CAN transceiver AN2005

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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